A Ku-band MMIC PLL Frequency Synthesizer

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Abstract **- A Ku-band PLL frequency synthesizer has been developed in a very compact configuration, incorporating two novel monolithic chips of GaAs MMIC and LSI. The MMIC includes a Ku-band VCO, a dual-output buffer amplifier, a balun and a dynamic/static prescaler. A very small chip size has been realized by the uni-planar MMIC configuration. The LSI includes a dual-modulus prescaler, programmable counters, and a PFC. The proposed synthesizer exhibits a tuning range broader than 1GHz and a phase noise of about -70 dBc/Hz at 1 kHz offset from the carrier.**

I. INTRODUCTION

Frequency synthesizers are commonly used to provide digital-tuning systems in communication equipment for lower frequencies such as UHF mobile radio. In microwave frequencies, however, frequency synthesizers are so complicated and expensive that their use is almost entirely confined to measurement systems.

This paper presents the trial development of a prototype GaAs MMIC PLL frequency synthesizer. The compact configuration of the synthesizer and its measured electric performance in the Ku-band frequencies are also described.

II. SYNTHESIZER DESIGN

The proposed synthesizer utilizes a direct division phase-locked loop (PLL)[1], shown in Fig.1, along with two constituent monolithic chips:

Chip I : GaAs MMIC :

voltage controlled oscillator (VCO)
+ buffer and power-splitter amplifier
+ CPW-to-slot transition (Balun)
+ high-speed prescaler

Chip II : GaAs LSI :

dual-modulus prescaler (÷4/÷5)
+ programmable counter (13bit)
+ phase / frequency comparator (PFC).

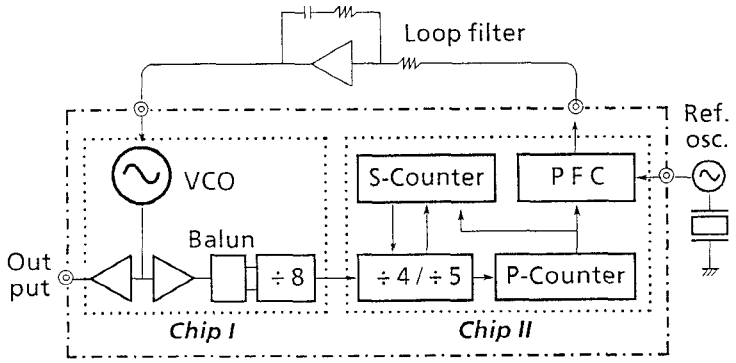

Fig.1: Synthesizer block diagram

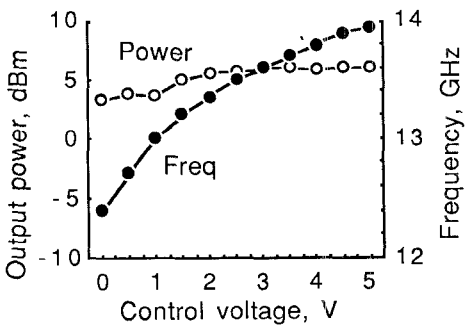

Fig.2: VCO tuning characteristics (with dual-output buffer)

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In this scheme, the VCO signal is amplified and split in two so that one goes to the output port and the other leads to the prescaler. The amplifier also prevents leakage of spurious signals from the digital circuits into the output port or the VCO.

Frequency division is executed with the 15GHz ÷ 8 prescaler and 2GHz programmable counters. The total division ratio was designed to be programmable from 160 to 65560, so that the reference frequency can be chosen from 200kHz to 100MHz through the specification of the frequency step.

A phase/frequency comparator (PFC) is utilized to maximize the capture range. Until the VCO frequency is locked, the PFC detects the frequency difference between the counter-output signal and the reference signal. After frequency locking, it detects their phase difference till the phase is locked.

In each circuit pattern, the *uni-planar* configuration [2] is utilized since it is advantageous for both a more compact layout and an easier fabrication process than a conventional microstrip configuration. To reduce chip size, all the matching circuits employ only lumped-constant elements--i.e., spiral inductors and MIM capacitors.

The whole system is integrated in a single package except for the loop filter and the reference oscillator.

III. Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) developed here consists of only monolithic elements and does not need any external resonators or tuners. It is an FET oscillator with a series feedback configuration. Another FET was shorted between its source and drain, and used as a varactor to vary the oscillation frequency. The varactor is coupled tightly to the FET, so that a wide tuning range is obtained, as shown in Fig.2. The circuit occupies as a small area as 0.5 x 0.8 mm in *Chip I* . By varying the control voltage from 0 to 5V, oscillation frequency varies from 12.4 to 13.9 GHz with an output power of more than 5dBm through the buffer amplifier described below.

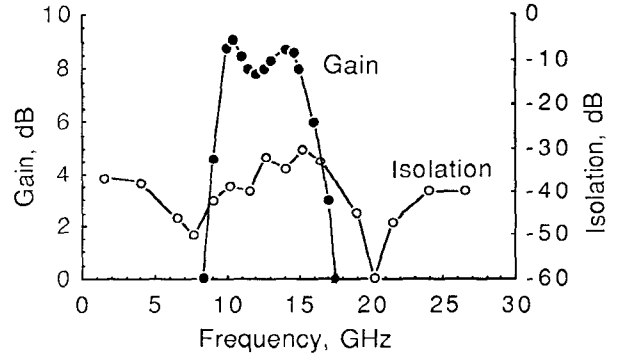

Fig.3: Dual-output buffer amplifier forward gain and isolation between the two output ports

IV. Buffer and Power Splitter Amplifier

A dual-output 2-stage amplifier is used as the buffer and power splitter. The first stage consists of two 100μm FETs with their gates connected to each other. The input matching circuit is common to the two amplifier blocks. A 200μm FET is used in the second stage of each block. The circuit is integrated into the small area of 1.5 x 1.6 mm in *Chip I*. The fabricated amplifier has a gain of more than 7dB for the two output ports in the 10-15GHz band, and an isolation of more than 30dB between the two output ports, as shown in Fig. 3.

V. High-Speed Prescaler

The newly developed high-speed prescaler is composed of a single-stage dynamic frequency divider[3] and a two-stage static frequency divider. Buffer FET logic is used in the dynamic frequency divider. Master-slave T-type flip-flops are used in the static divider.

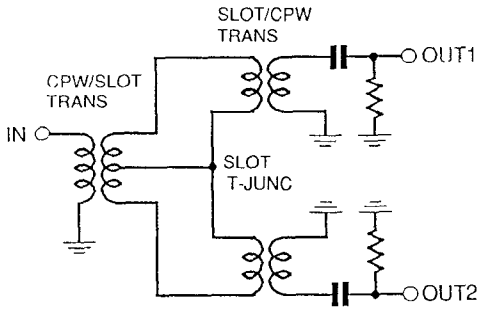

Fig.4: Balun using CPW-SLOT transition

In front of the dynamic frequency divider, a novel uni-planar balun is used to convert a single input clock to complementary clocks. As shown in Fig.4, it is composed of transitions[4] between a CPW (unbalanced mode) and a slot line (balanced mode) and branches of a slot line. Unlike a rat-race circuit, this balun includes no frequency-sensitive elements. It offers very satisfactory broadband matching performance as shown in Fig.5.

The measured maximum operating frequency of this ÷8 prescaler with the balun exceeds 15GHz as shown in Fig.6.

VI. Programmable Counter and PFC

The second innovative chip (*Chip II*) includes a ÷4/÷5 dual-modulus prescaler, 11-bit (pulse) and 2-bit (swallow) synchronous counters and a phase/frequency comparator (PFC). This consists of 3000 FETs and measures 3.1x3.2mm. A low-power source-coupled FET logic[5] is used as the basic circuit for its high speed and good functionality. The prescaler and counters are programmable to provide a division ratio from 20 to 8195. The measured maximum operating frequency exceeds 4 GHz, as shown in Fig.7.

VII. Synthesizer Performance

All the circuits described above occupy much less area than conventional ICs, as shown in Fig.8. They are integrated in two chips and mounted in a 11 x 23 mm flat package shown in Fig.9. The synthesizer can be assembled with an external lag-lead loop filter and a reference crystal oscillator.

An example of the measured output spectrum is shown in Fig.10, where the reference frequency is 85 MHz and the frequency division ratio is 160. The marker in the near-carrier spectrum (upper photograph) indicates that the SSB noise density is about -70dBc/Hz at 1kHz offset from the 13.6GHz carrier.

Spurious subharmonic f/2, f/4 and f/8 signals are found in the DC-20GHz span spectrum (lower photograph). Since these subharmonics are far from and much below the desired signal, they

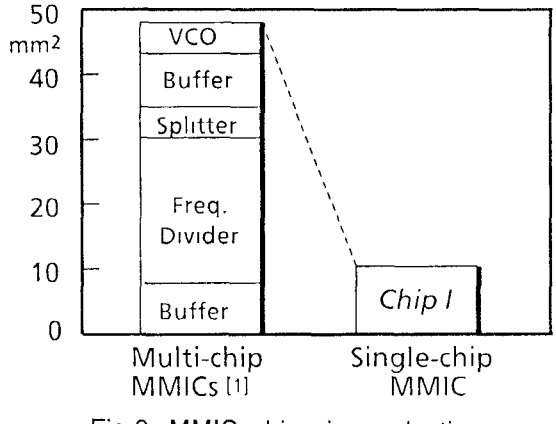

Fig.8: MMIC chip size reduction

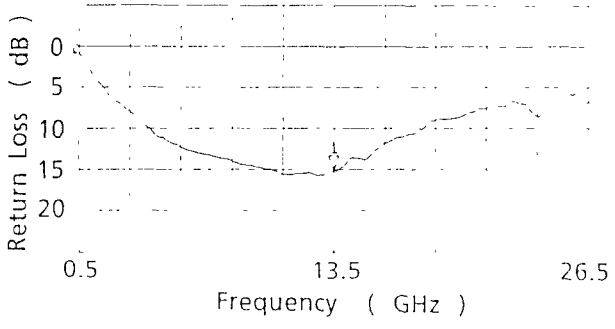

Fig.5: Balun input return loss

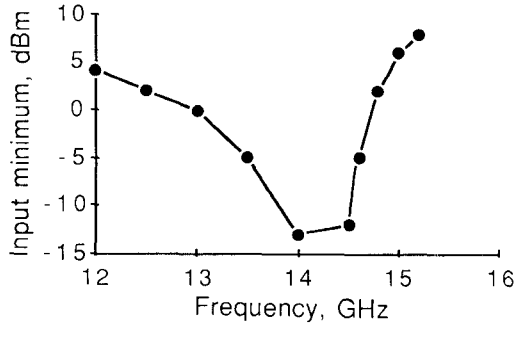

Fig 6: Prescaler with balun input sensitivity

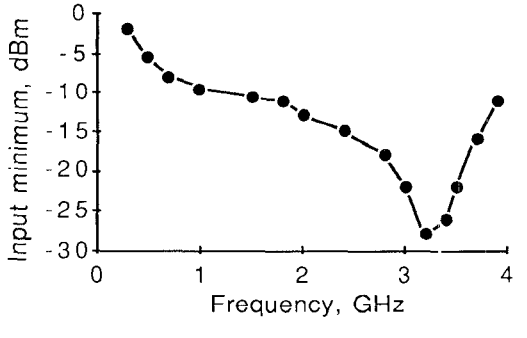

Fig.7: Dual-modulus prescaler input sensitivity

could be eliminated through a rough high-pass filter.

The flatness of the output level has also been measured. The maximum ripple exhibited is less than 2 dBpp in the full tuning band, as shown in Fig.11.

VIII. CONCLUSIONS

A miniaturized Ku-band PLL frequency synthesizer has been developed, incorporating two inovative chips of GaAs MMIC and LSI. The analog and digital circuits needed for the synthesizer function have all been integrated in these two chips except for the loop filter. The assembled synthesizer has a tuning range broader than 1GHz in the Ku-band within 2dBpp flatness. In spite of the low-Q monolithic circuitry, the SSB phase noise is as low as -70dBc/Hz. Since the proposed synthesizer is both compact and rugged, it should contribute to the development of very small digital-tuning microwave transmitters and receivers that could be applied in various radio communication equipment.

ACKNOWLEDGMENT

The authors wish to thank Dr.H.Yamamoto, Dr.T.Sugeta, H.Kato and M.Hirayama for helpful discussions and encouragement. They also wish to thank Dr.M.Ohhata and M.Togashi for digital circuit design, F.Ishitsuka for packaging, and T.Nakagawa for PLL circuit design and assembly.

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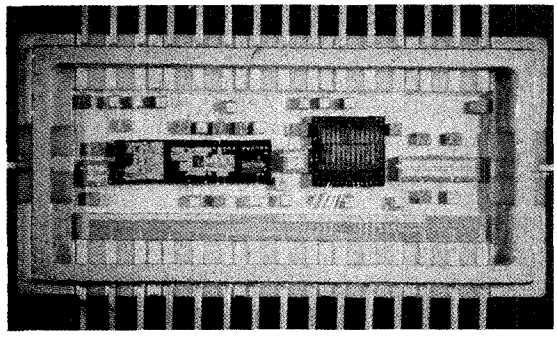
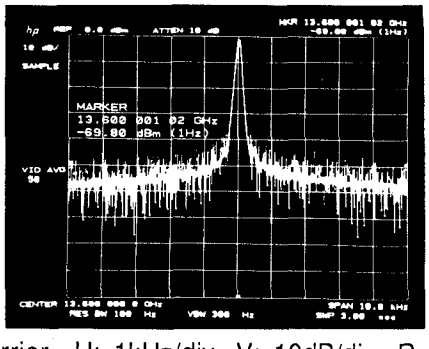
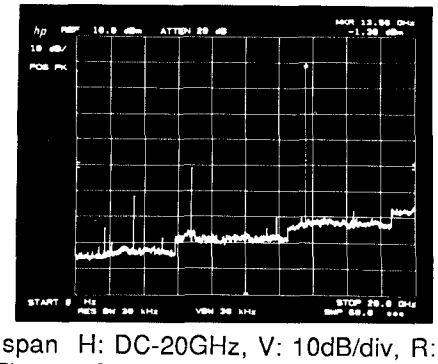


Fig.9: Synthesizer with the cover removed
The package measures 11 x 23 mm.



Near carrier H: 1kHz/div, V: 10dB/div, R: 100Hz



Wide span H: DC-20GHz, V: 10dB/div, R: 1MHz
Fig.10: Synthesizer output spectrum

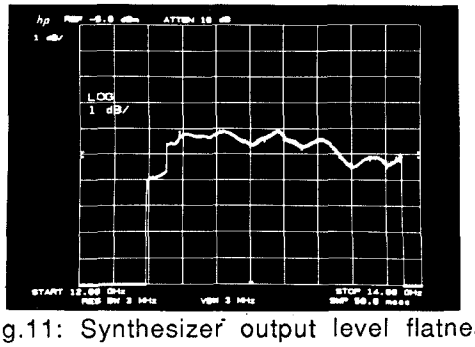


Fig.11: Synthesizer output level flatness
H: 12-14GHz, V: 1dB/div